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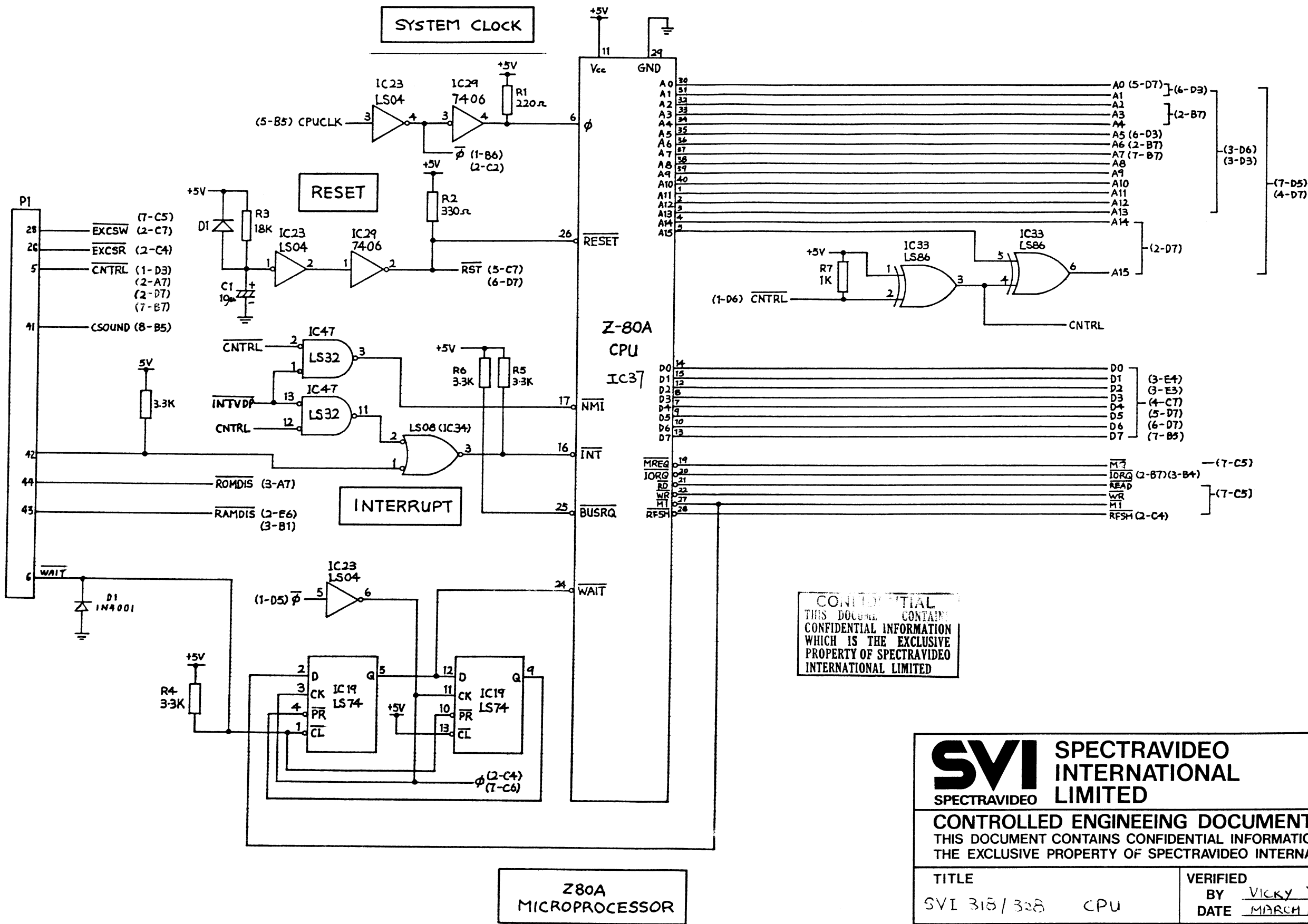
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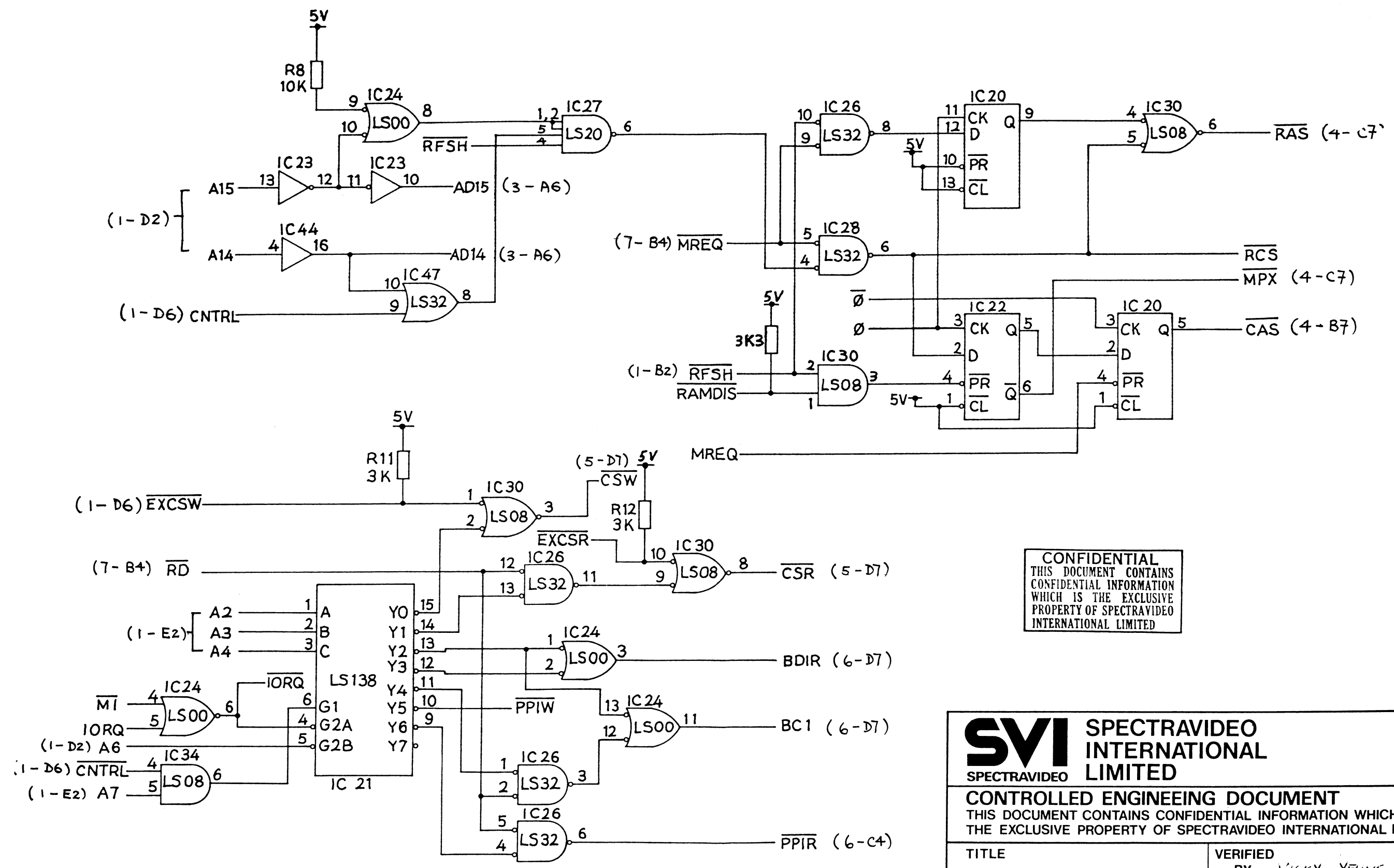


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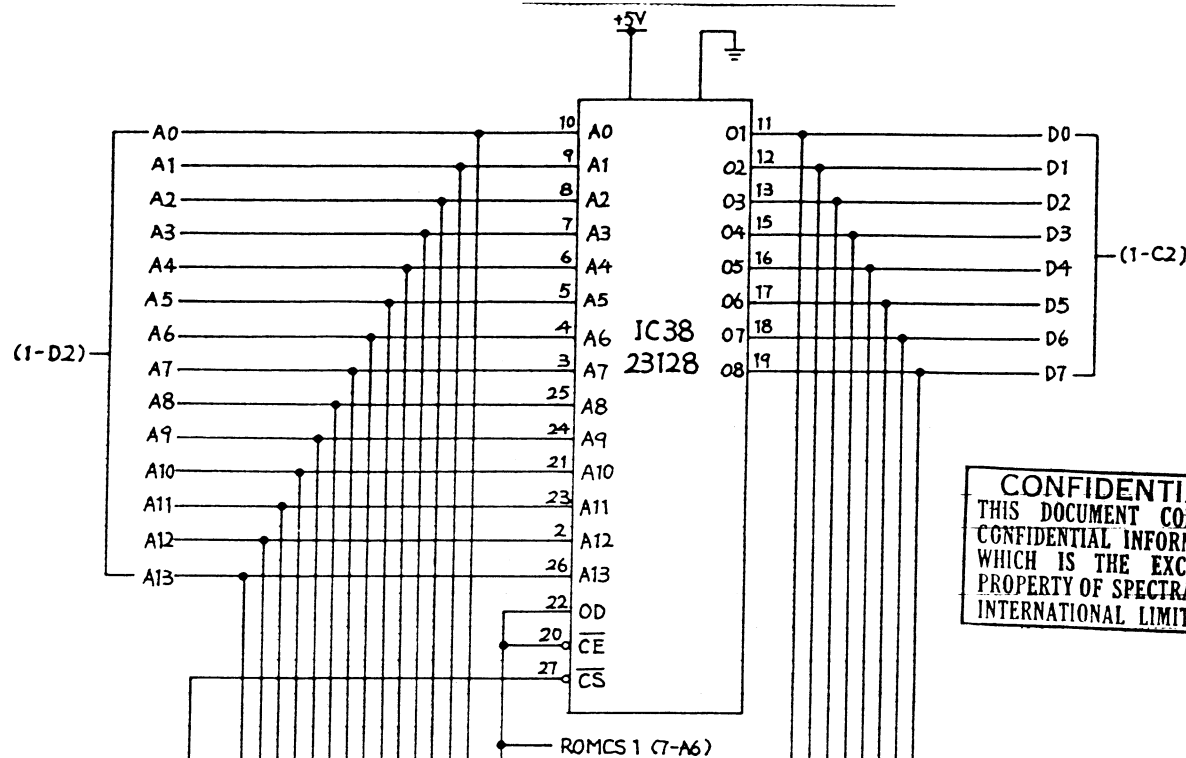
TITLE SVI 318/328 CPU	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH 1984</u>
DOCUMENT NO STM-001-A	VERSION NO 1.5 SHEET 1 OF 12



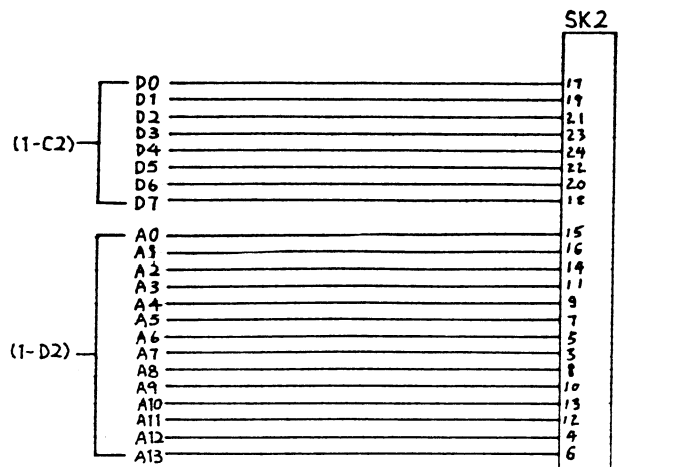
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TITLE DECODE LOGIC	VERIFIED BY <u>VICKY YEUNG VY</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO STM-002-A	VERSION NO 1.5 SHEET 2 OF 12

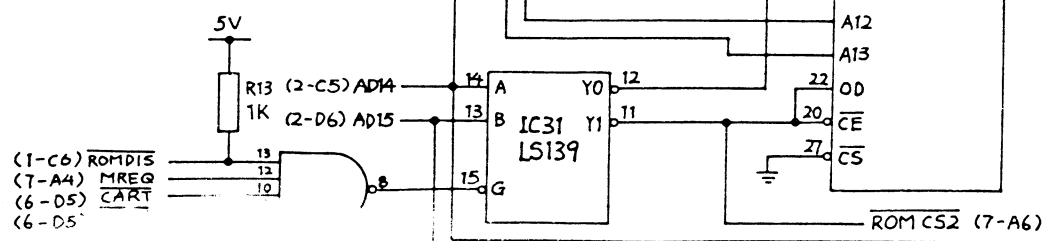
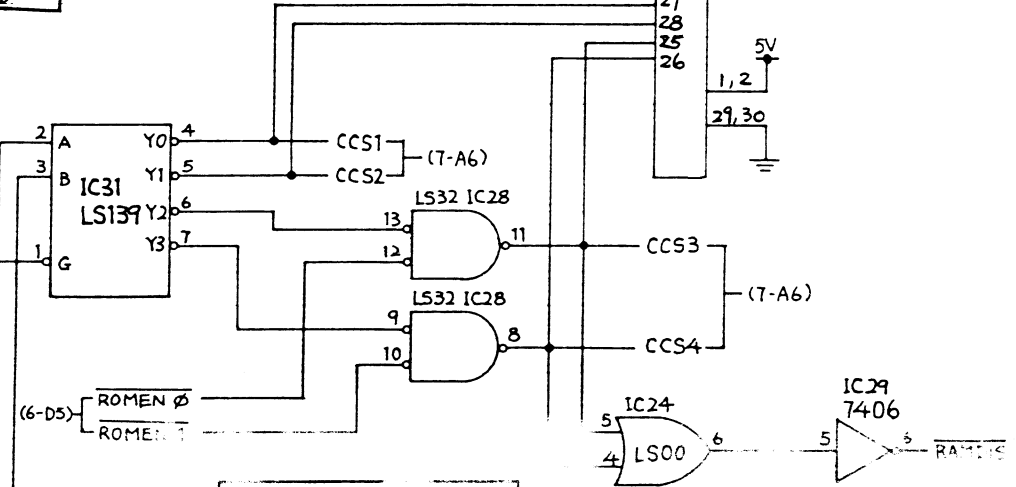
MASS ROM MEMORY



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MEMORY CONTROL



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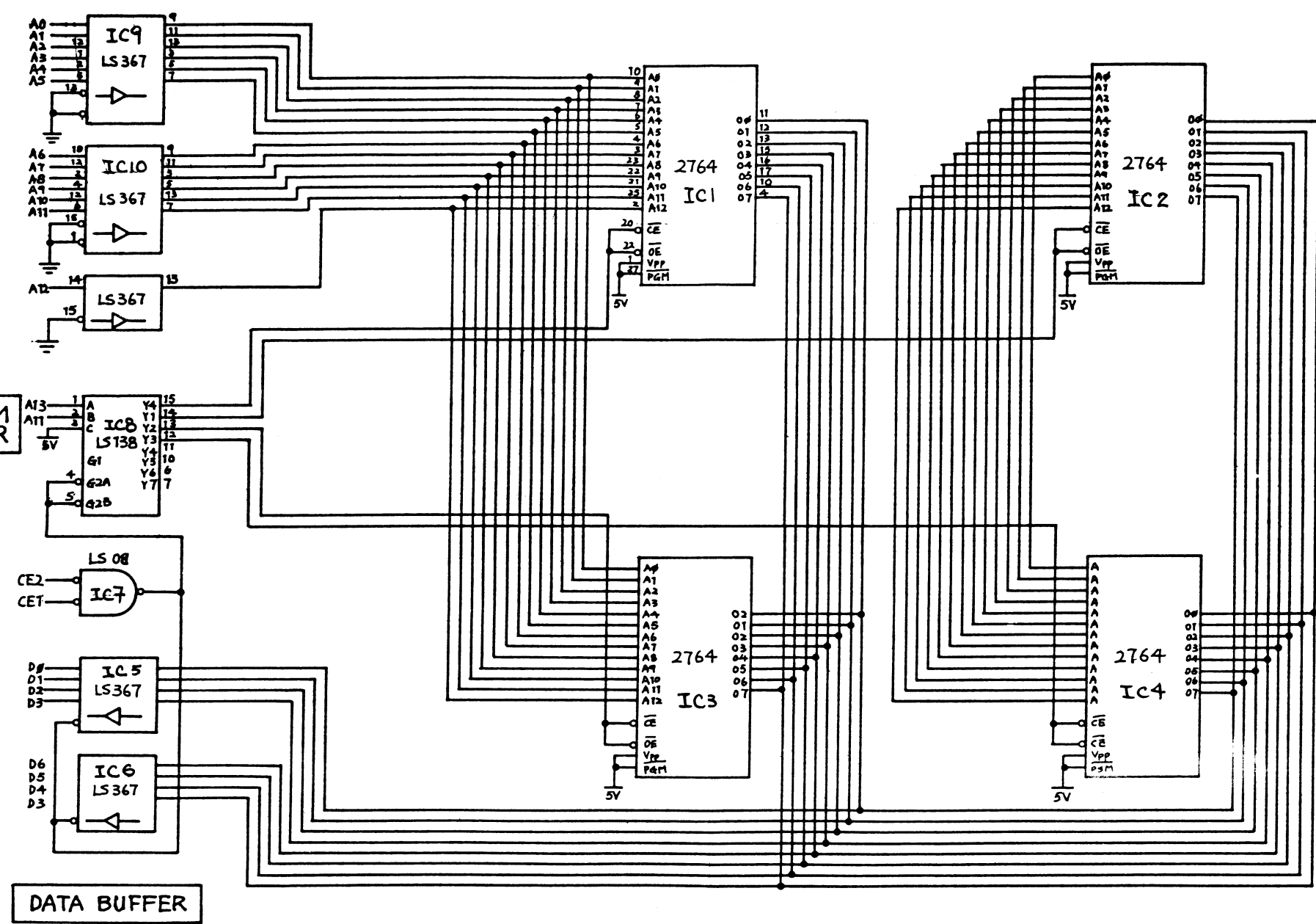
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TITLE MASS ROM & MEMORY CONTROL	VERIFIED BY <u>WELLY YEUNG</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO SIM-003-A	VERSION NO 1.5 SHEET 3 OF 12

ADDRESS BUFFER

32KB SYSTEM EPROM

EPROM DECODER



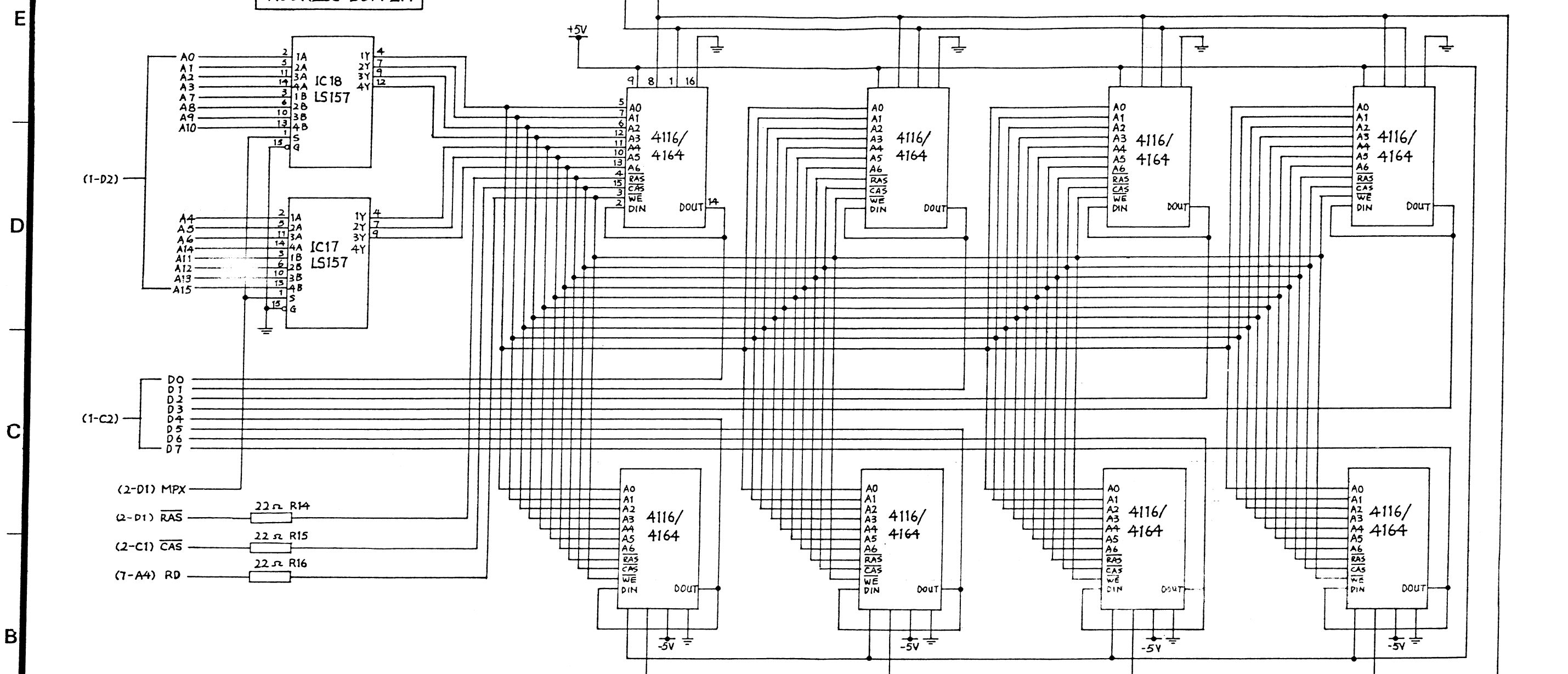
DATA BUFFER

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TITLE EPROM & MEMORY CONTROL	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH 1984</u>
DOCUMENT NO STM-004-A	VERSION NO 1.5 SHEET 3 OF 12



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TITLE	VERIFIED
16K OR 64K USER MEMORY	BY <i>VICKY YEUNG V.Y.</i>
	DATE <i>MARCH, 1984</i>

DOCUMENT NO	VERSION NO	SHEET OF
SFM - 005 - A	1.5	4 OF 12

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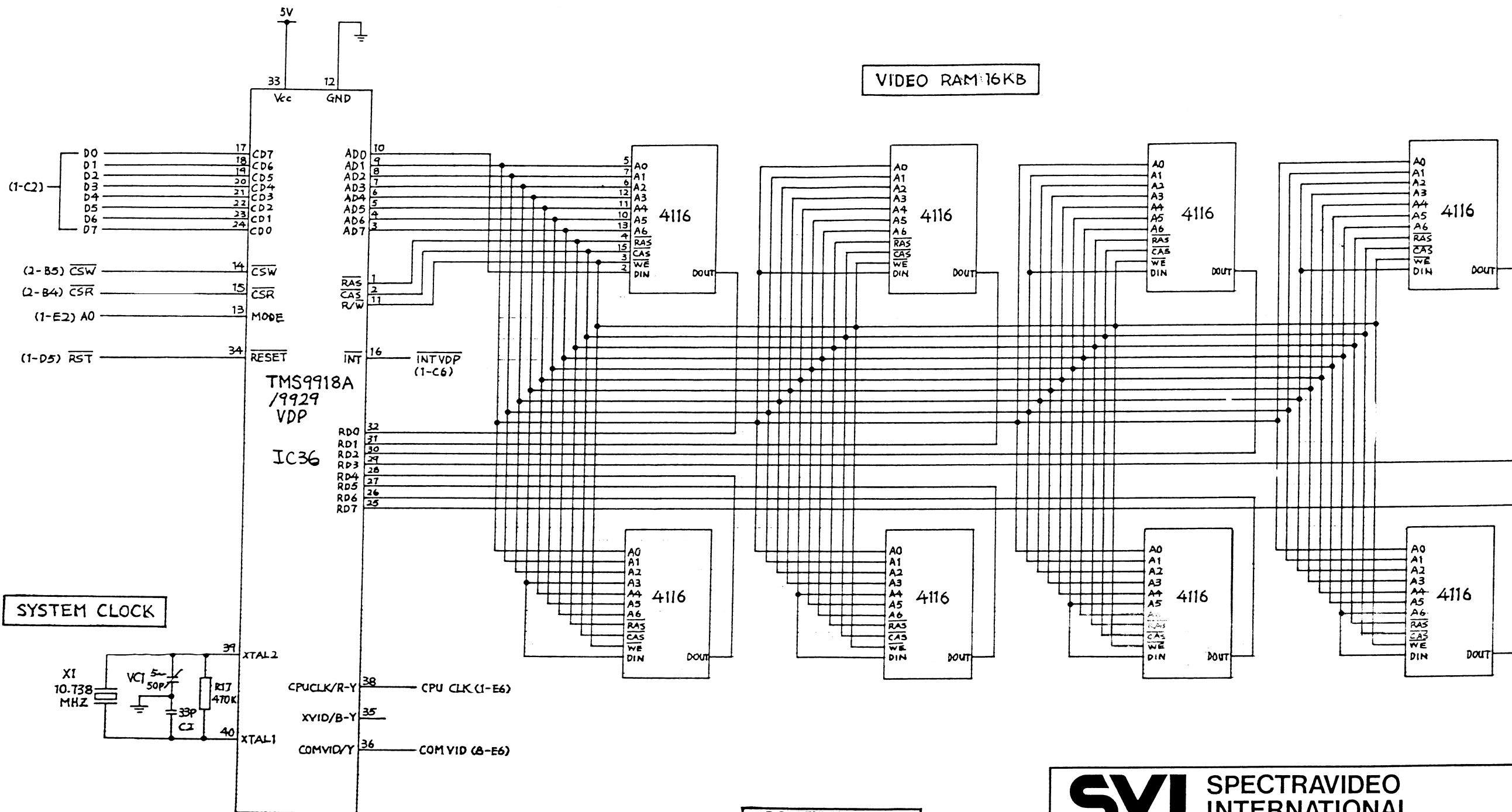
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SYSTEM CLOCK

VIDEO RAM 16KB

TMS9918A / 9929
VIDEO DISPLAY PROCESSOR

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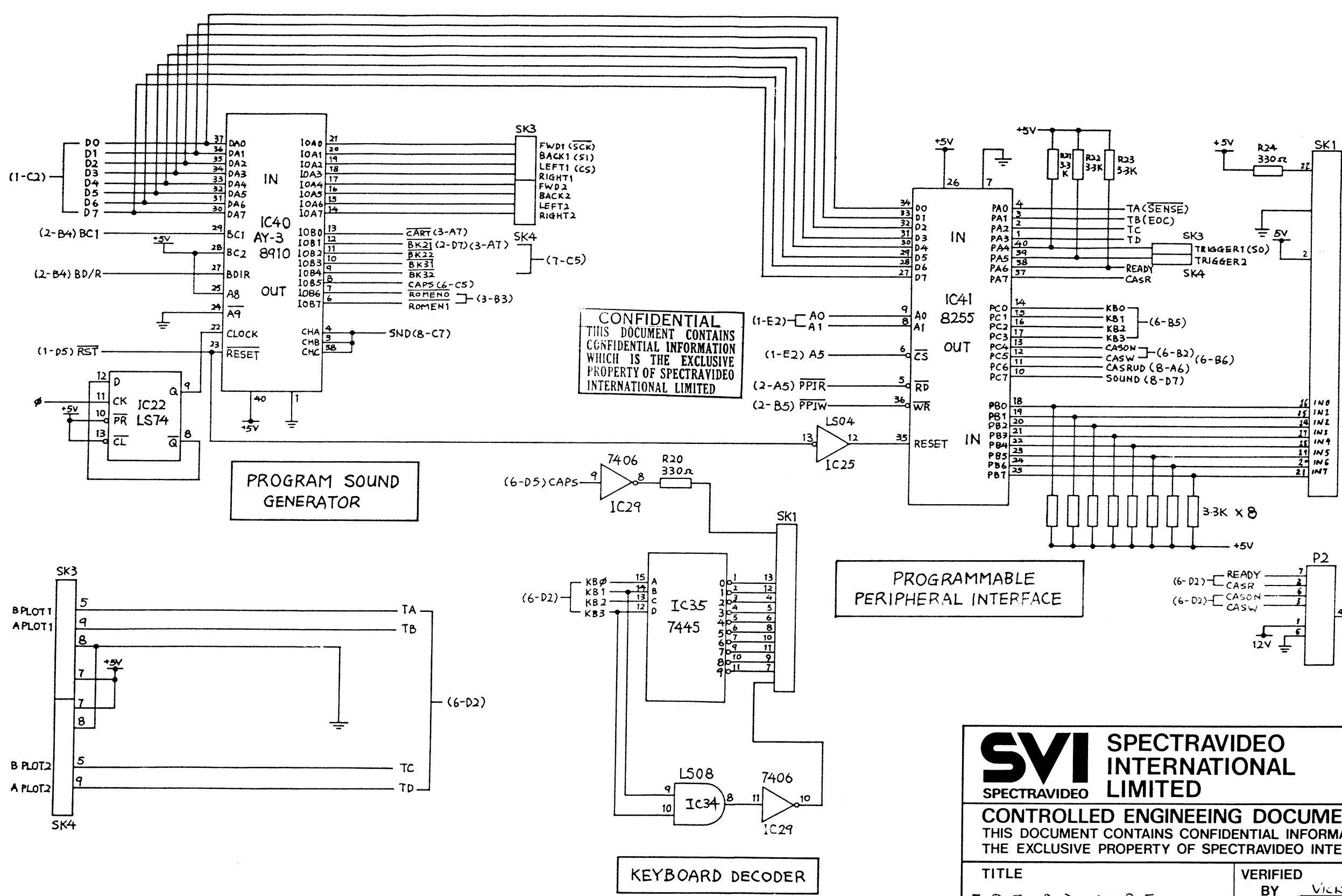
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TITLE VDP & 16K VIDEO RAM	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO STM-006-A	VERSION NO 1.5
	SHEET 5 OF 12

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TITLE INPUT AND OUTPUT	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH 1984</u>
DOCUMENT NO STM-007-A	VERSION NO 1.5 SHEET 6 OF 12

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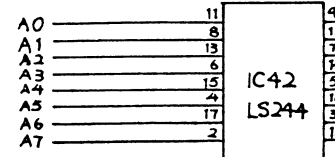
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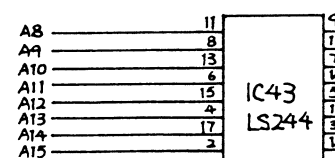
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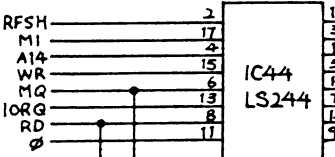
ADDRESS BUFFER



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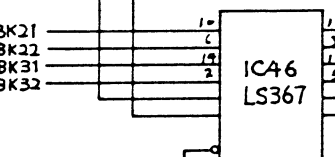


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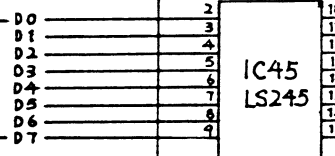


CONTROL BUFFER

(6-D5)



(1-C2)



DATA BUFFER

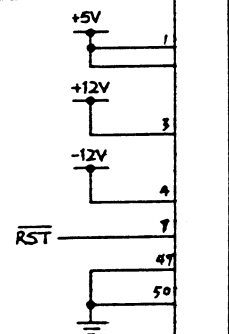
IC25 LS04

LS04 IC25

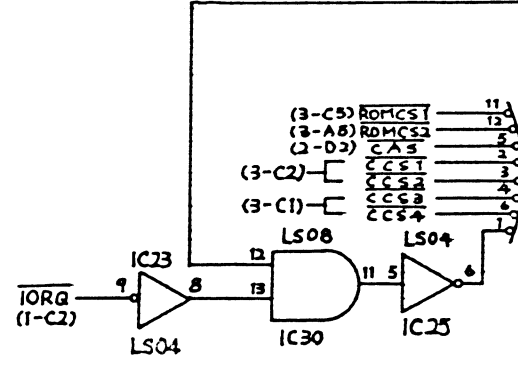
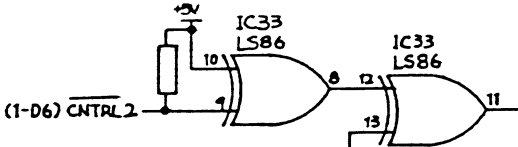
LS04 IC25

RD (4-BT)

MREQ (3-A1) (2-B2)



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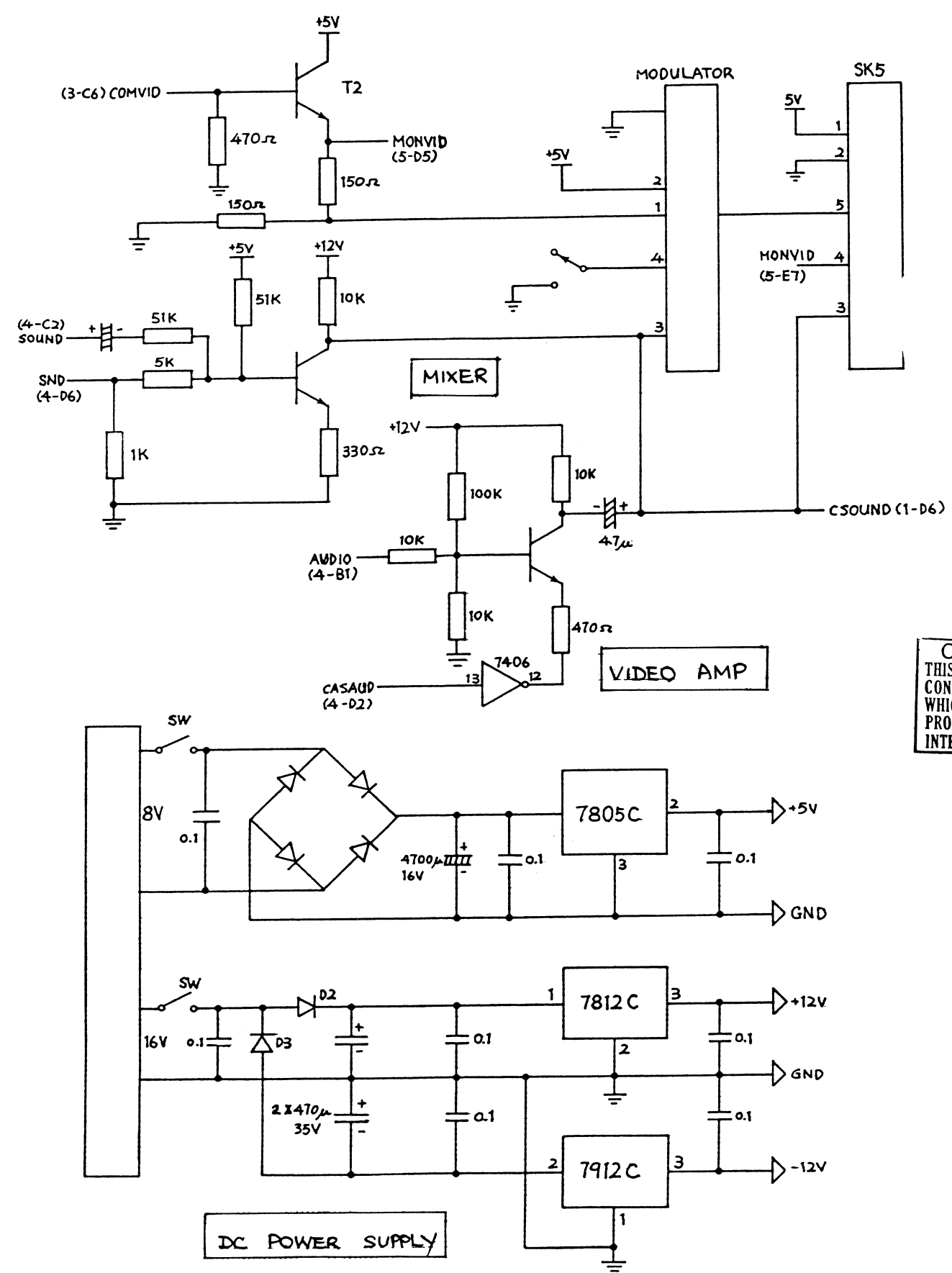
BUFFER CONTROL

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TITLE SYSTEM BUS BUFFER	VERIFIED BY <u>VICKY YOUNG V.Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO STM-008-A	VERSION NO 1.5 SHEET 7 OF 12

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PIN	NAME	PIN	NAME
1	+5V	2	CNTRL2
3	+12V	4	-12V
5	CNTRL1	6	WAIT
7	RST	8	CPU CLK
9	A15	10	A14
11	A13	12	A12
13	A11	14	A10
15	A9	16	A8
17	A7	18	A6
19	A5	20	A4
21	A3	22	A2
23	A1	24	A0
25	RFSH	26	EXCSR
27	MI	28	EXCSW
29	WR	30	MREQ
31	TORQ	32	RD
33	D0	34	D1
35	D2	36	D3
37	D4	38	D5
39	D6	40	D7
41	CSOUND	42	INT
43	RAMDIS	44	ROMDIS
45	BK32	46	BK31
47	BK22	48	BK21
49	GND	50	GND

EXT. BUS PIN ASSIGNMENT

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TITLE COMVIDEO & POWER SUPPLY	VERIFIED BY VICKY YEUNG V.S.
DATE MARCH 1984	
DOCUMENT NO STM-007-A	VERSION NO 1.5
	SHEET OF 8 OF 12

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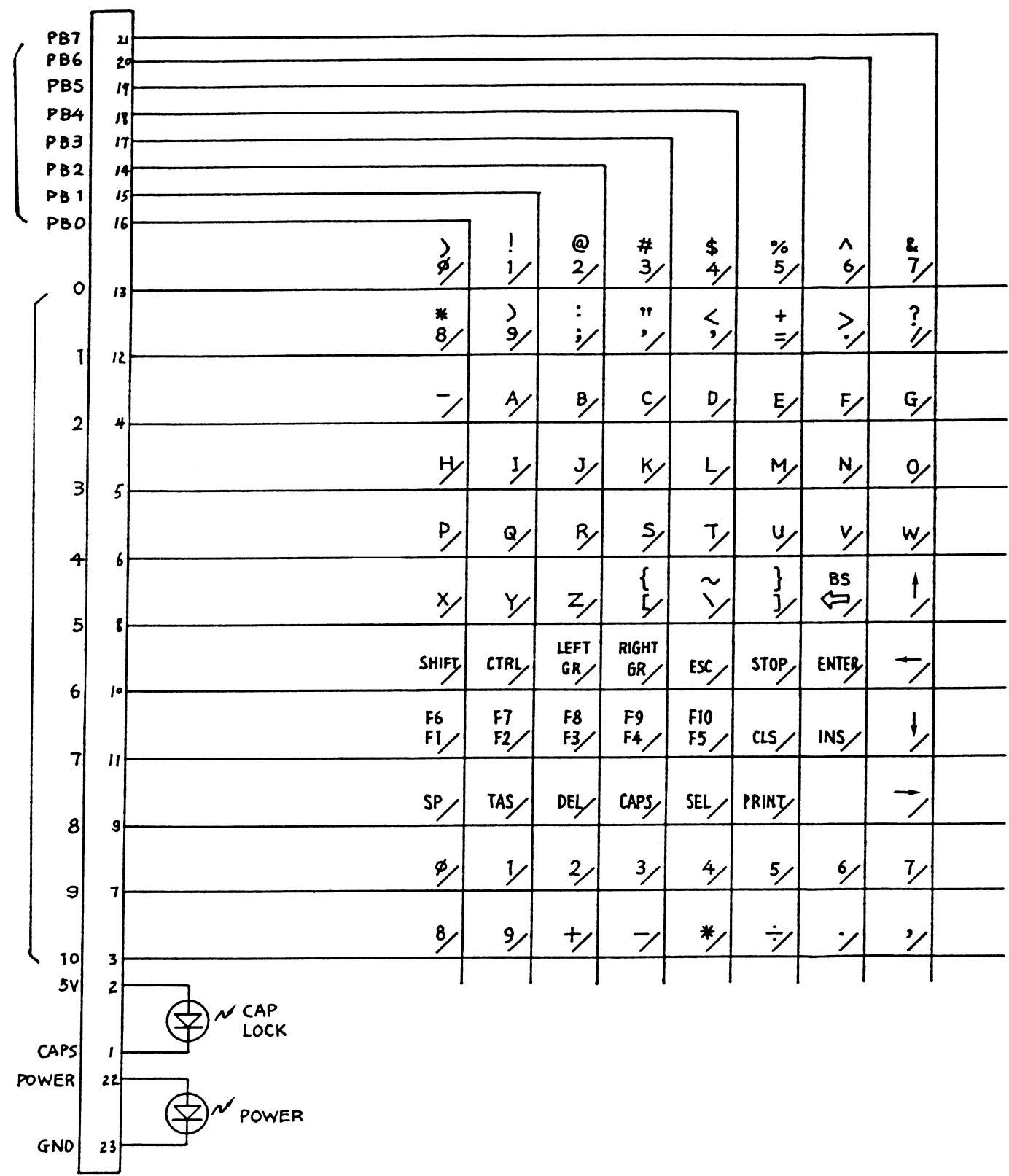
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INPUT

OUTPUT



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TITLE ASCII KEYBOARD	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH 1984</u>
DOCUMENT NO STM-010-A	VERSION NO 1.5 SHEET 9 OF 12

PIN	NAME	PIN	NAME
1	+5V	2	+5V
3	A7	4	A12
5	A6	6	A13
7	A5	8	A8
9	A4	10	A9
11	A3	12	A11
13	A10	14	A2
15	A0	16	A1
17	D0	18	D7
19	D1	20	D6
21	D2	22	D5
23	D3	24	D4
25	CCS3	26	CCS4
27	CCS1	28	CCS2
29	Gnd.	30	Gnd.

GAME CARTRIDGE

PIN	NAME
1	12V
2	CASR
3	CASW
4	AUDIO
5	Gnd.
6	\overline{ME}
7	READY

CASSETTE

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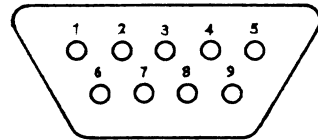
PIN	NAME
1	CAPS
2	5V
3	OUTPUT 10
4	OUTPUT 2
5	OUTPUT 3
6	OUTPUT 4
7	OUTPUT 9
8	OUTPUT 5
9	OUTPUT 8
10	OUTPUT 6
11	OUTPUT 7
12	OUTPUT 1
13	OUTPUT 0
14	INPUT 2
15	INPUT 1
16	INPUT 0
17	INPUT 3
18	INPUT 4
19	INPUT 5
20	INPUT 6
21	INPUT 7
22	POWER
23	Gnd.
24	
25	

KEYBOARD

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TITLE I/O PORT DESCRIPTION	VERIFIED BY <u>VICKY YEUNG V Y</u> DATE <u>MARCH 1984</u>
DOCUMENT NO <u>SEM-011-A</u>	VERSION NO <u>1.5</u> SHEET <u>10</u> OF <u>12</u>

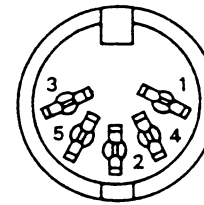
PIN	NAME
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2	BACKWARD/SI
3	LEFT/CS
4	RIGHT/SENCTR
5	SENSE
6	TRIGGER
7	+5V
8	GND
9	EOC

SK3 JOYSTICK 1



PIN	NAME
1	+5V
2	GND.
3	AUDIO
4	MONITOR VIDEO
5	RF VIDEO

SK5 VIDEO & AUDIO



PIN	NAME
1	FORWARD/SCK
2	BACKWARD/SI
3	LEFT/CS
4	RIGHT/SENCTR
5	SENSE
6	TRIGGER
7	+5V
8	GND
9	EOC

SK4 JOYSTICK 2

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TITLE I/O PORT DESCRIPTION	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH 1984</u>
DOCUMENT NO STM-012-A	VERSION NO 1.5 SHEET 11 OF 12

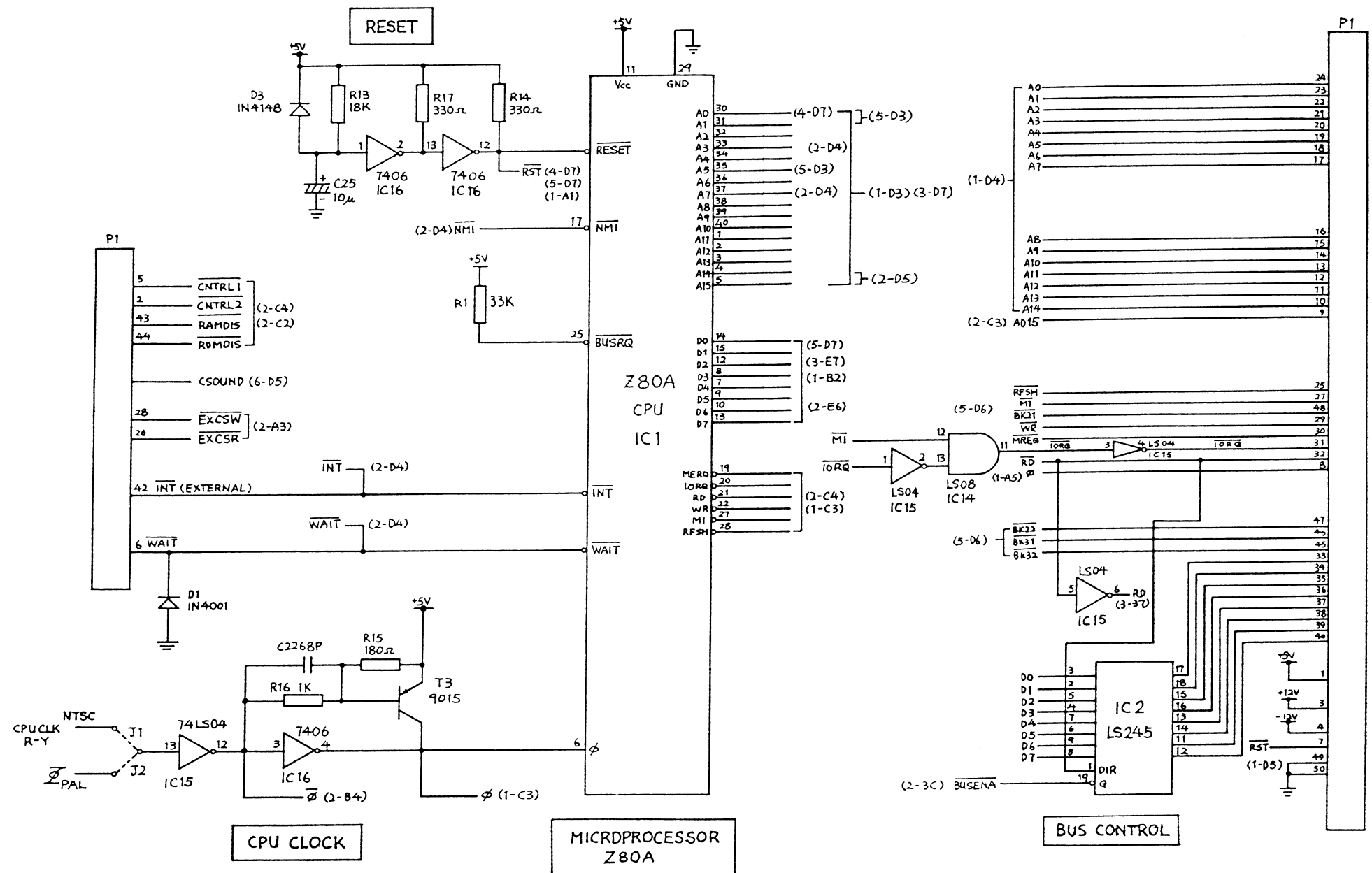
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SVI-318MKII-CPU

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TITLE MKII CPU	VERIFIED BY <i>VICKY YOUNG</i> DATE <i>MARCH 1984</i>
DOCUMENT NO STM-014-A	VERSION NO 1.0 SHEET OF 1

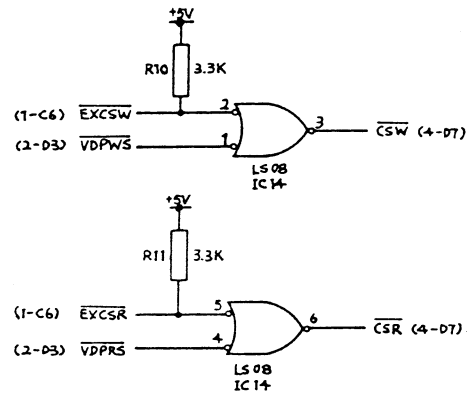
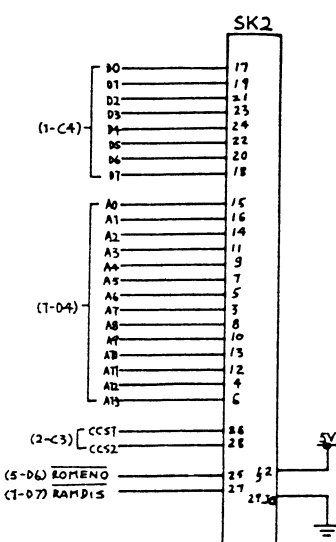
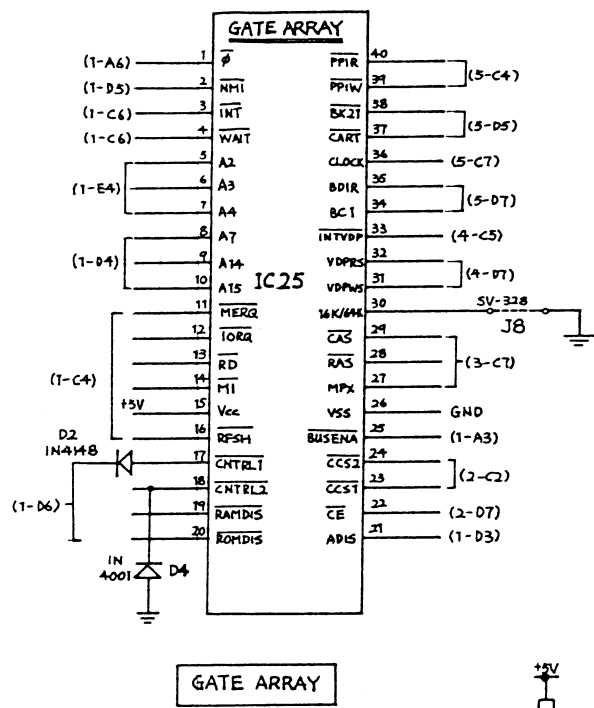
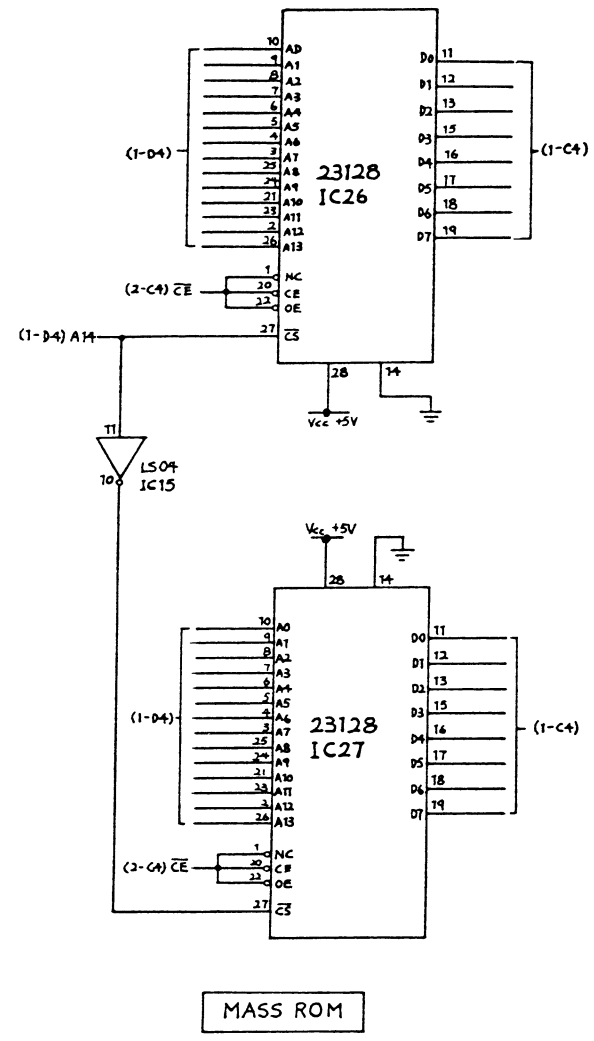
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TITLE MASS ROM & GATE ARRAY	VERIFIED BY <u>VICKY YELING V.Y.</u> DATE <u>MARCH 1984</u>
DOCUMENT NO STM-015-A	VERSION NO 1.0 SHEET OF 2

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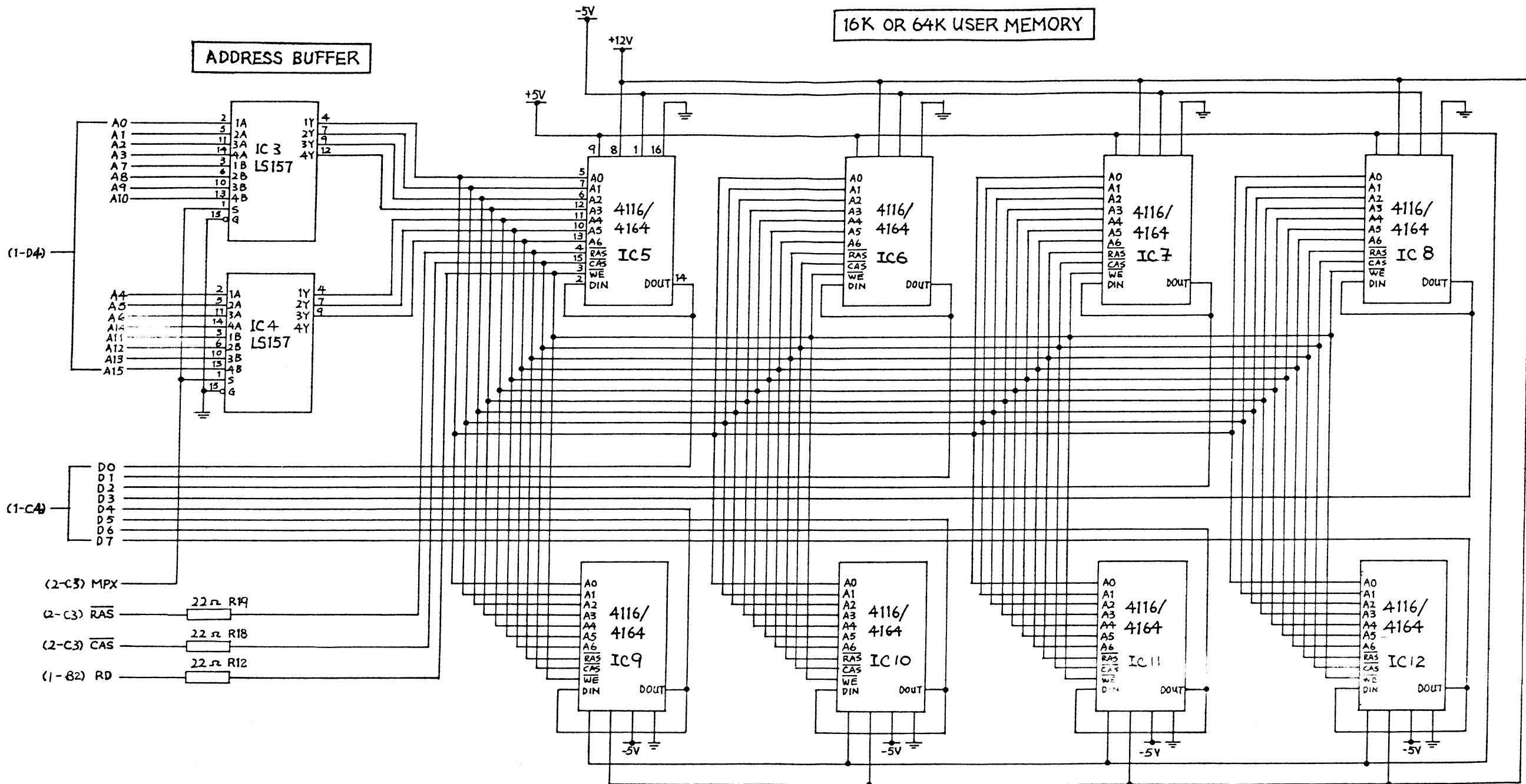
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ADDRESS BUFFER

16K OR 64K USER MEMORY



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TITLE 16K OR 64K USER MEMORY	VERIFIED BY VICKY YEUNG V.Y.
	DATE MARCH 1984
DOCUMENT NO STM-016-A	VERSION NO 1.0
	SHEET OF 3

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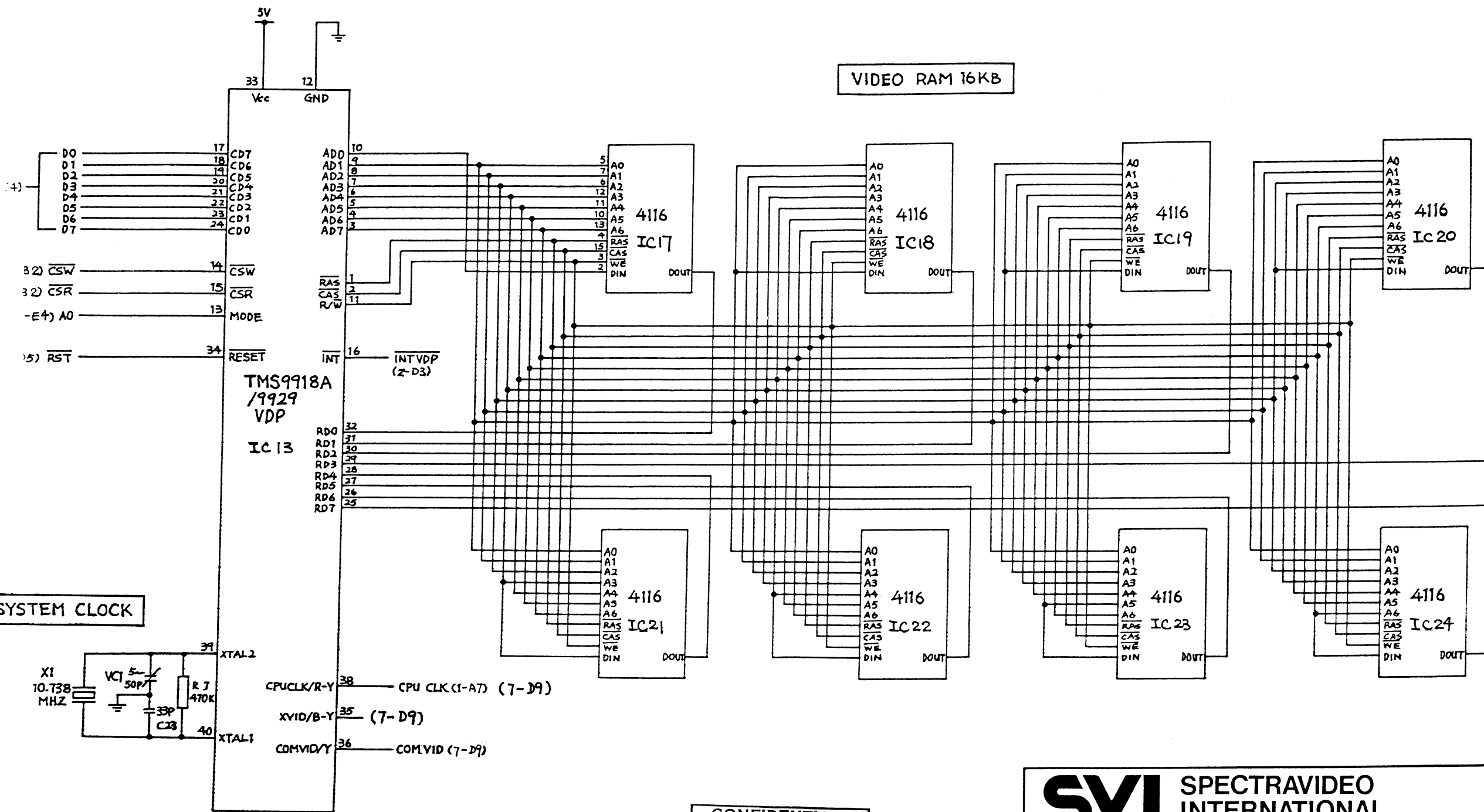
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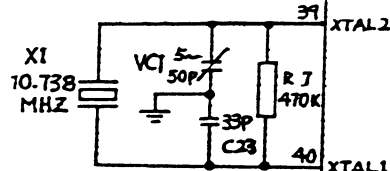
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SYSTEM CLOCK



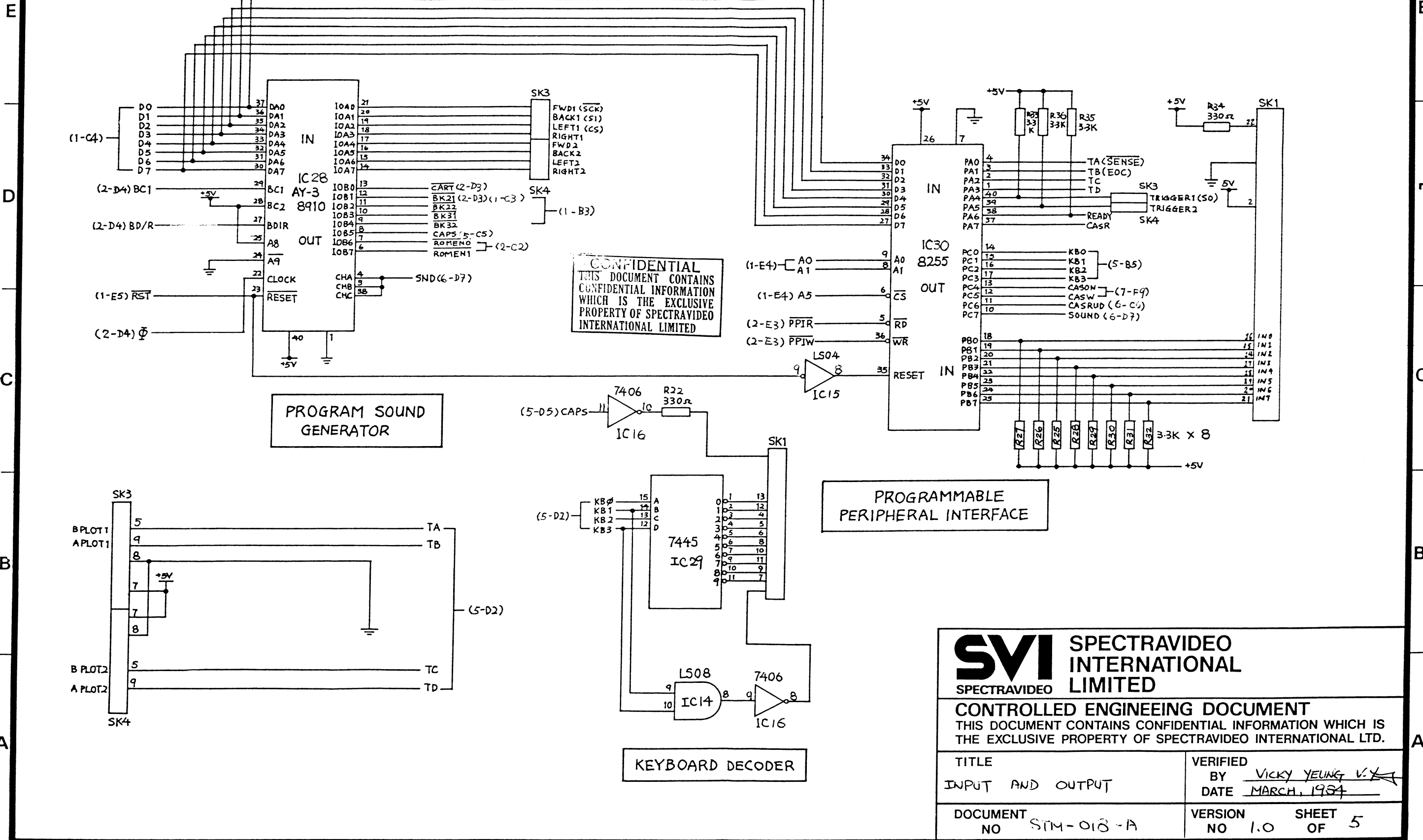
TMS-9918A / 9929
VIDEO DISPLAY PROCESSOR

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TITLE VDP & 16K VIDEO RAM	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO <u>STM-017-A</u>	VERSION NO <u>1.0</u> SHEET OF <u>4</u>



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PROGRAM SOUND
 GENERATOR

PROGRAMMABLE
 PERIPHERAL INTERFACE

KEYBOARD DECODER

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TITLE INPUT AND OUTPUT	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO STM-018-A	VERSION NO 1.0 SHEET OF 5

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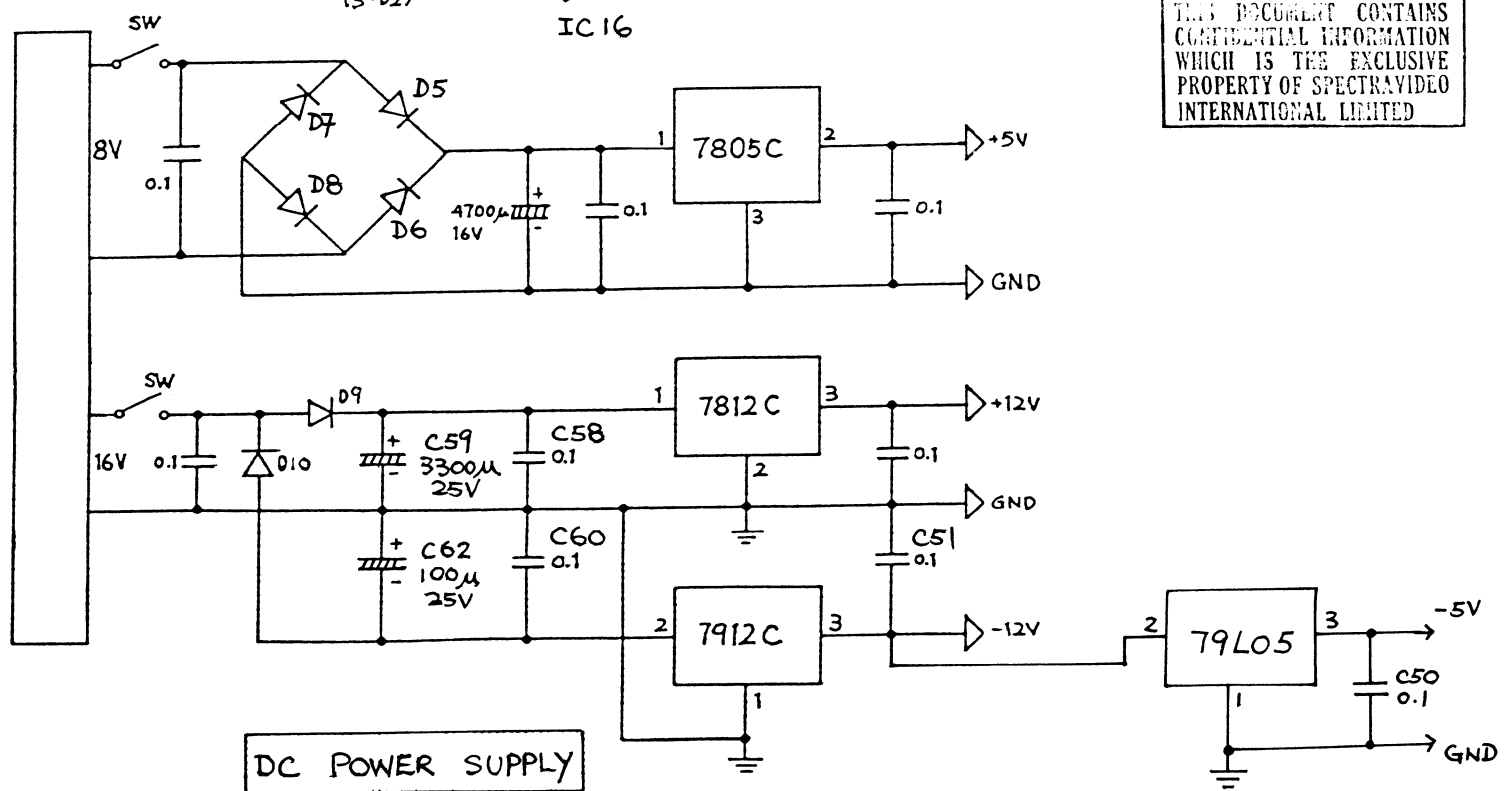
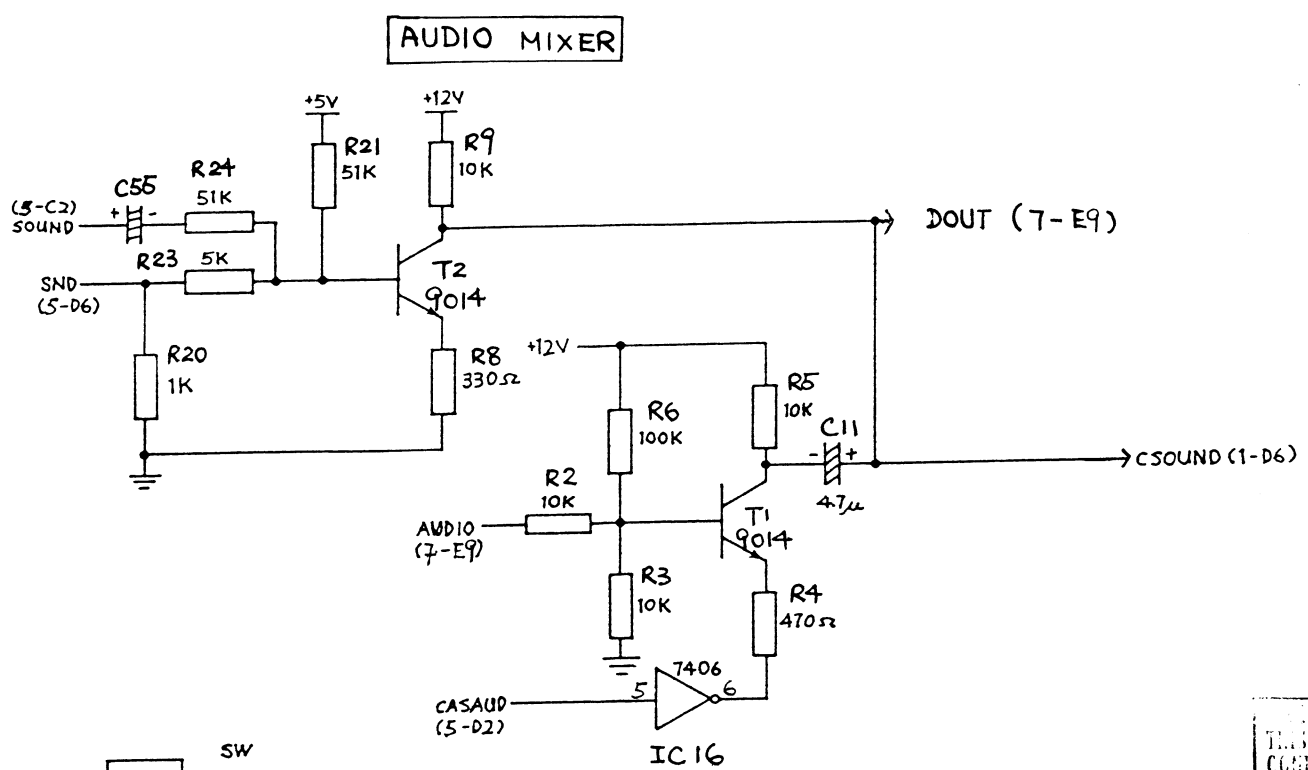
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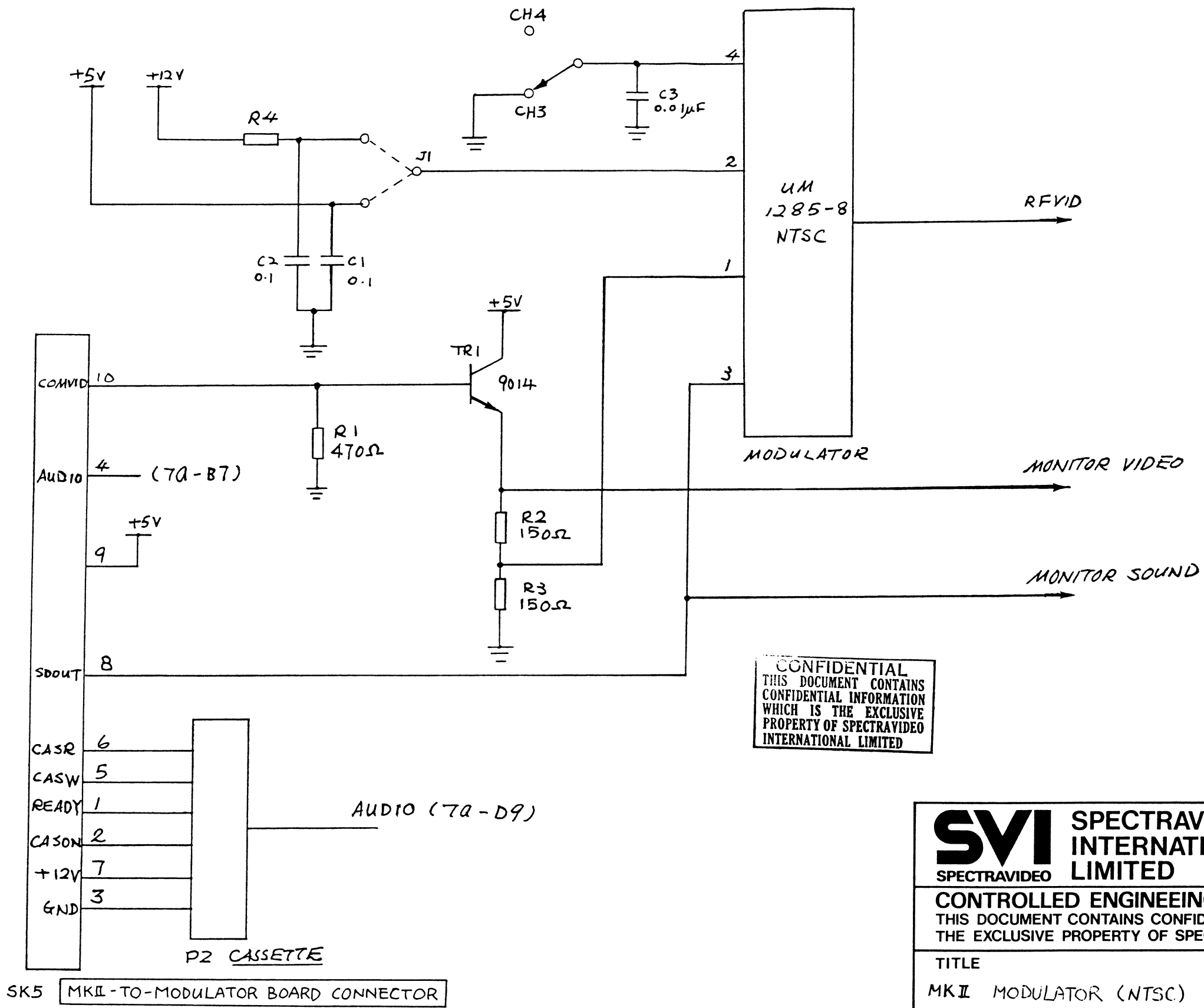
PIN	NAME	PIN	NAME
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3	+12V	4	-12V
5	CNTRL1	6	WAIT
7	RST	8	CPU CLK
9	A15	10	A14
11	A13	12	A12
13	A11	14	A10
15	A9	16	A8
17	A7	18	A6
19	A5	20	A4
21	A3	22	A2
23	A1	24	A0
25	RFSH	26	EXCSR
27	MI	28	EXCSW
29	WR	30	MREQ
31	IORQ	32	RD
33	D0	34	D1
35	D2	36	D3
37	D4	38	D5
39	D6	40	D7
41	CSOUND	42	INT
43	RAMDIS	44	ROMDIS
45	BK32	46	BK31
47	BK22	48	BK21
49	GND	50	GND

EXT. BUS PIN ASSIGNMENT

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TITLE AUDIO MIXER & POWER SUPPLY	VERIFIED BY <i>VICKY YOUNG V. Y.</i> DATE <i>MARCH, 1984</i>
DOCUMENT NO STM-019-A	VERSION NO 1.0 SHEET OF 6



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TITLE MKII MODULATOR (NTSC)	VERIFIED BY <i>VICKY YEUNG V.Y.</i> DATE <i>MARCH, 1984</i>
DOCUMENT NO STM-020-A	VERSION NO 1.0 SHEET OF 7a

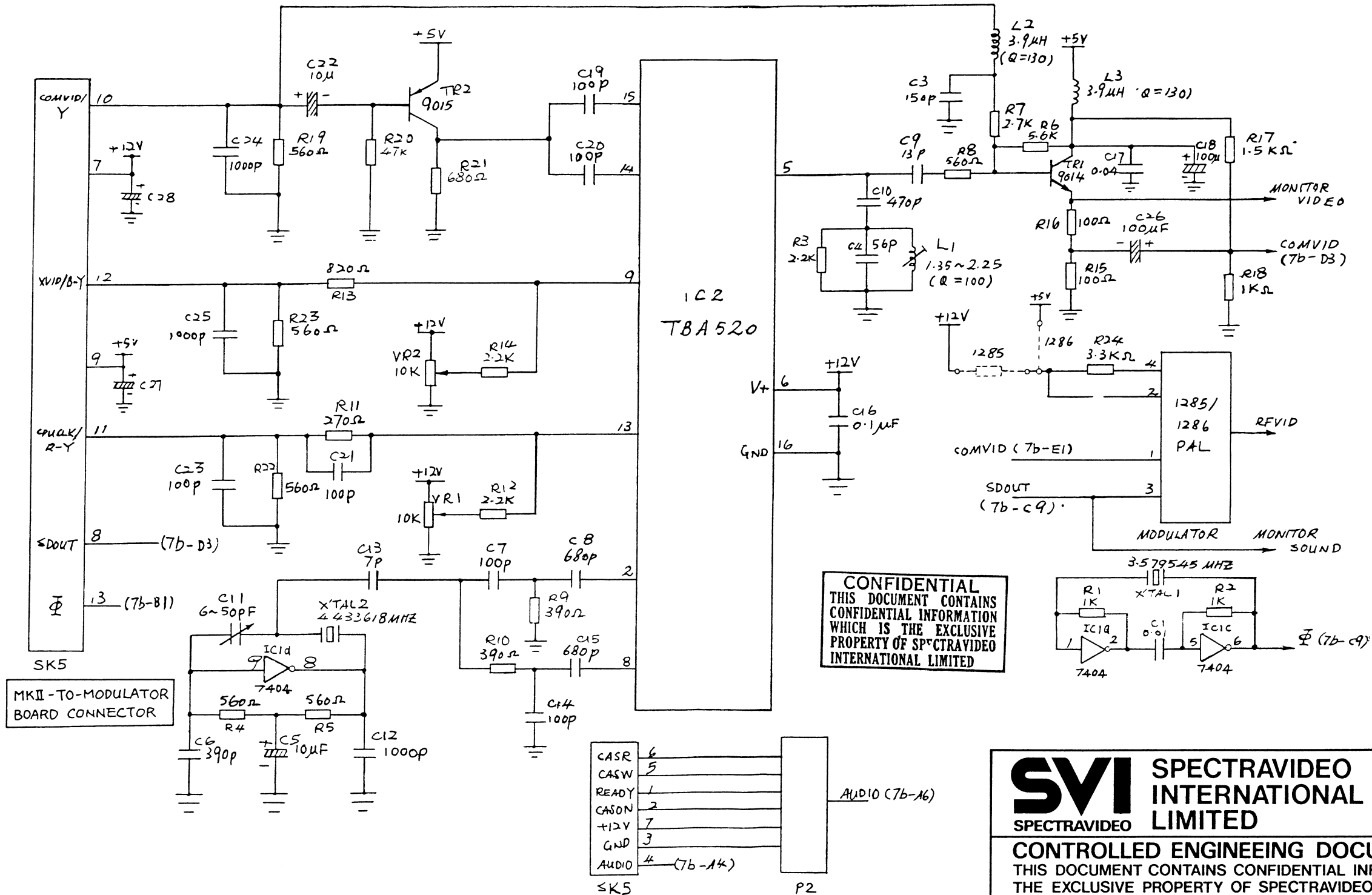
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TITLE MKII MODULATOR (PAL)	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH 1984</u>
DOCUMENT NO STM-021-A	VERSION NO 1.0 SHEET OF 7b

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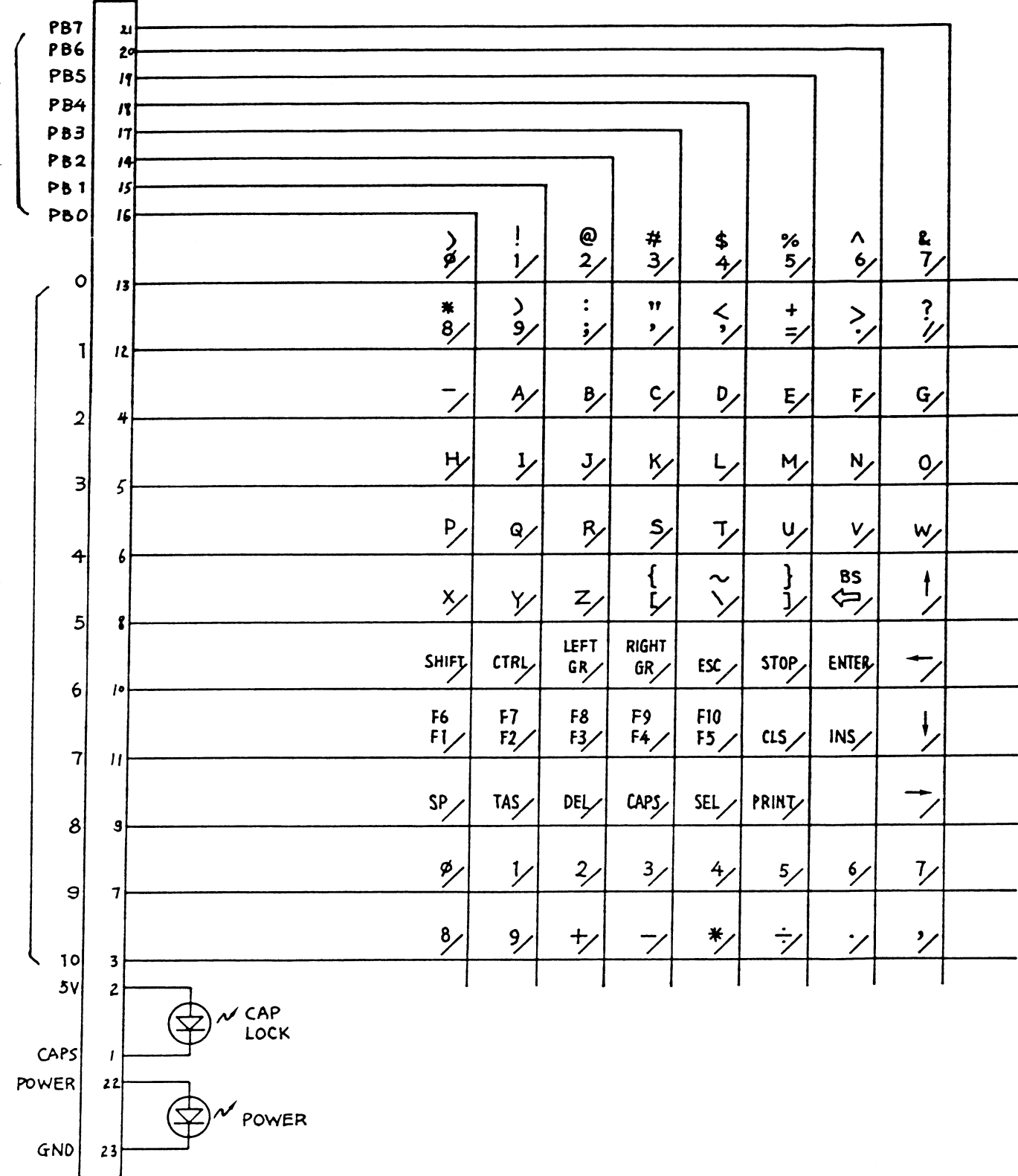
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INPUT

OUTPUT



SK1 KEYBOARD

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TITLE ASCII KEYBOARD	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO STM-022-A	VERSION NO 1.0 SHEET OF 8a

E

D

C

B

A

PIN	NAME	PIN	NAME
1	+5V	2	+5V
3	A7	4	A12
5	A6	6	A13
7	A5	8	A8
9	A4	10	A9
11	A3	12	A11
13	A10	14	A2
15	A0	16	A1
17	D0	18	D7
19	D1	20	D6
21	D2	22	D5
23	D3	24	D4
25	CCS3	26	CCS4
27	CCS1	28	CCS2
29	Gnd.	30	Gnd.

GAME CARTRIDGE

PIN	NAME
1	12V
2	CASR
3	CASW
4	AUDIO
5	Gnd.
6	ME
7	READY

CASSETTE

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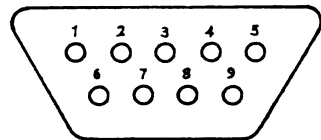
PIN	NAME
1	CAPS
2	5V
3	OUTPUT 10
4	OUTPUT 2
5	OUTPUT 3
6	OUTPUT 4
7	OUTPUT 9
8	OUTPUT 5
9	OUTPUT 8
10	OUTPUT 6
11	OUTPUT 7
12	OUTPUT 1
13	OUTPUT 0
14	INPUT 2
15	INPUT 1
16	INPUT 0
17	INPUT 3
18	INPUT 4
19	INPUT 5
20	INPUT 6
21	INPUT 7
22	POWER
23	Gnd.
24	
25	

KEYBOARD

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DOCUMENT NO <u>STM-023-A</u>	VERSION NO <u>1.0</u> SHEET OF <u>8b</u>

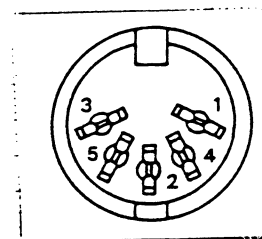
PIN	NAME
1	FORWARD / SCK
2	BACKWARD / SI
3	LEFT / CS
4	RIGHT / SENCTR
5	SENSE
6	TRIGGER
7	+5V
8	GND
9	EOC

SK3 JOYSTICK 1



PIN	NAME
1	FORWARD / SCK
2	BACKWARD / SI
3	LEFT / CS
4	RIGHT / SENCTR
5	SENSE
6	TRIGGER
7	+5V
8	GND.
9	EOC

SK4 JOYSTICK 2



PIN	NAME
1	+5V
2	GND.
3	AUDIO
4	MONITOR VIDEO
5	RF VIDEO

SK5 VIDEO & AUDIO

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DOCUMENT NO STM-024-A	VERSION NO 1.0 SHEET OF 80

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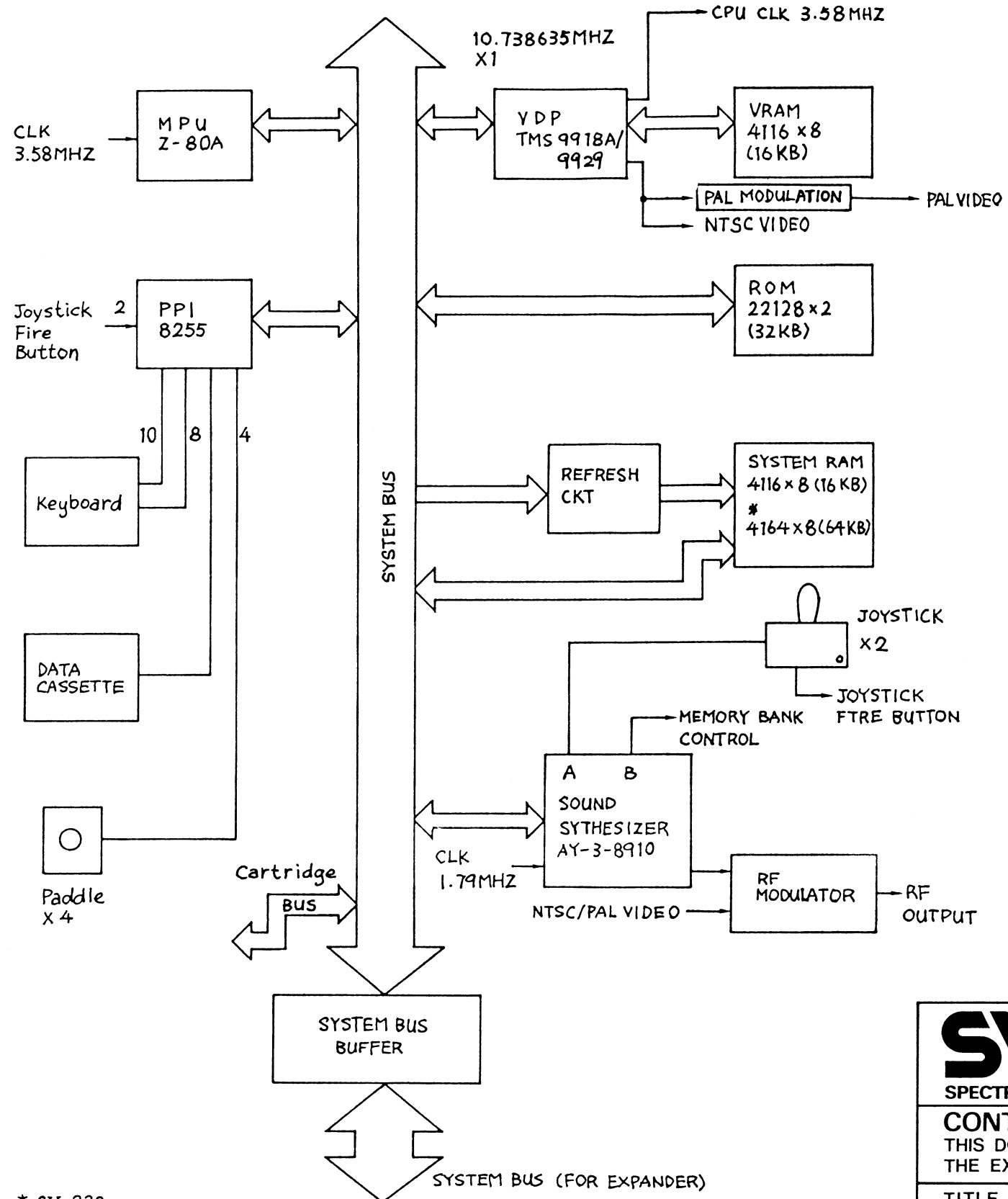
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* SV-328

SVI318, 328 or MKII SYSTEM ARCHITECTURE

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TITLE SVI 318/328 or MKII SYSTEM ARCHITECTURE	VERIFIED BY <u>VICKY YEUNG V. Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO <u>SVI-025-A</u>	VERSION NO <u>1.0</u> SHEET OF <u>1</u>

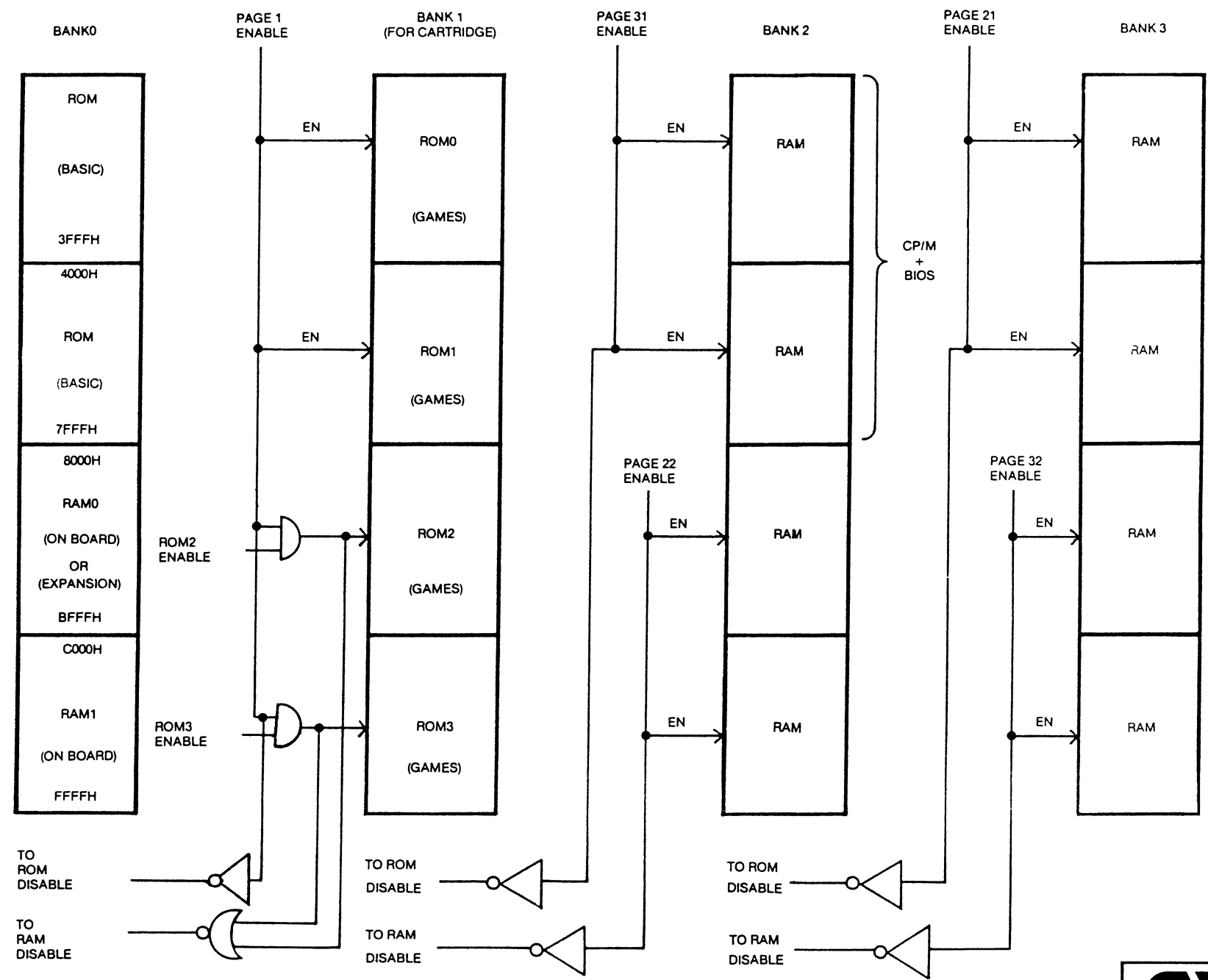
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TITLE SVI 318/325 CP/MK II MEMORY MAP BLOCK DIAGRAM	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO <u>STM-026-A</u>	VERSION NO <u>1.0</u> SHEET OF <u>2</u>

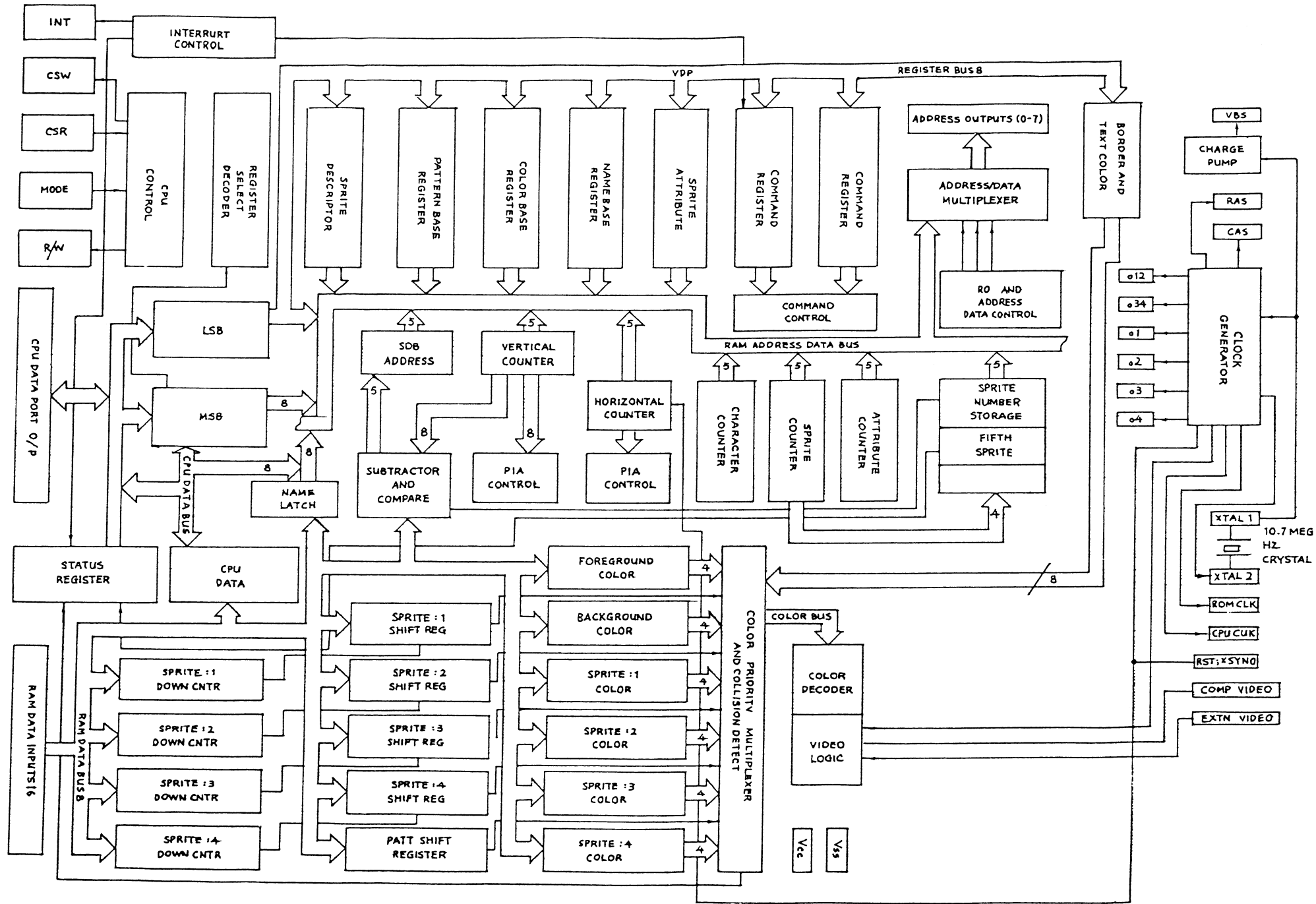
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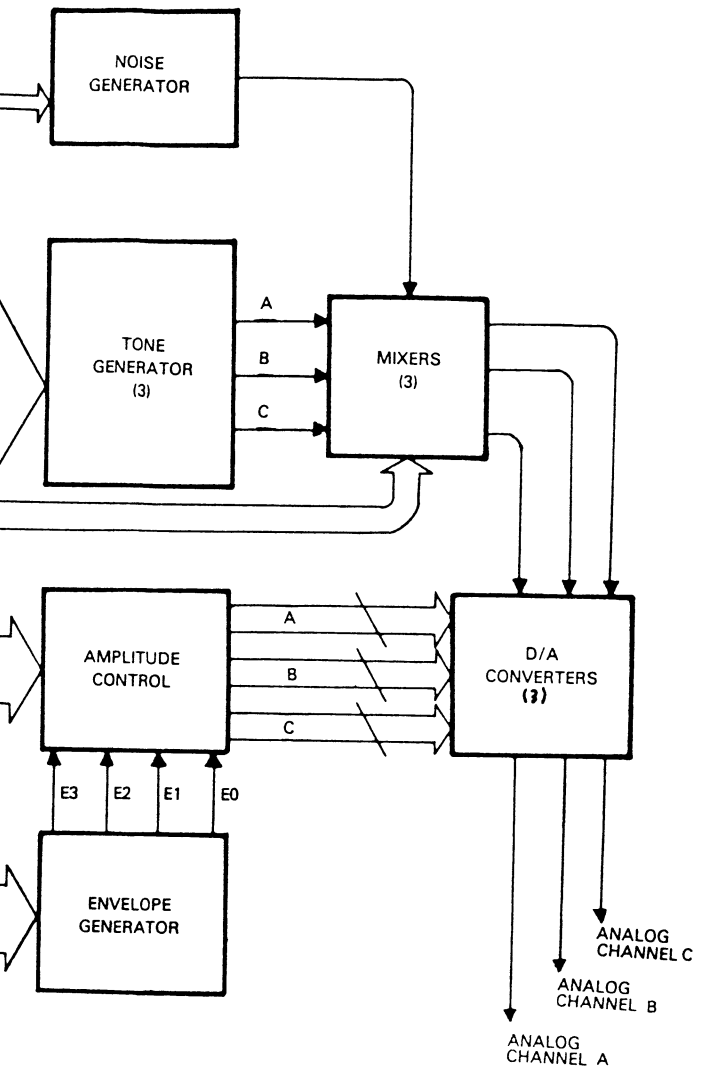
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TITLE TMS 9918A/9929 VIDEO DISPLAY PROCESSOR BLOCK DIAGRAM	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO <u>STM-027-A</u>	VERSION NO <u>1.0</u> SHEET OF <u>3</u>

PSG BLOCK DIAGRAM

REGISTER	BIT	B7	B6	B5	B4	B3	B2	B1	B0
R0		8-BIT Fine Tune A							
R1	Channel A Tone Period	8-BIT Fine Tune A				4 BIT Coarse Tune A			
R2	Channel B Tone Period	8-BIT Fine Tune B				4 BIT Coarse Tune B			
R3	Channel C Tone Period	8-BIT Fine Tune C				4 BIT Coarse Tune C			
R4	Channel A Tone Period	8-BIT Fine Tune B				4 BIT Coarse Tune B			
R5	Channel B Tone Period	8-BIT Fine Tune C				4 BIT Coarse Tune C			
R6	Noise Period	8-BIT Fine Tune A					4 BIT Coarse Tune A		
R7	Enable	IN/OUT		Noise			Tone		
		I0B	I0A	C	B	A	C	B	A
R8	Channel A Amplitude	8-BIT Fine Tune A			M	L3	L2	L1	L0
R9	Channel B Amplitude	8-BIT Fine Tune B			M	L3	L2	L1	L0
R10	Channel C Amplitude	8-BIT Fine Tune C			M	L3	L2	L1	L0
R11	Envelope Period	8 BIT Fine Tune E							
R12	Envelope Period	8 BIT Coarse Tune E							
R13	Envelope Shape/Cycle	8-BIT Fine Tune A				CONT.	ATT.	ALT.	HOLD

REGISTERED ARRAY
(14 READ/WRITE
CONTROL REGISTERS)

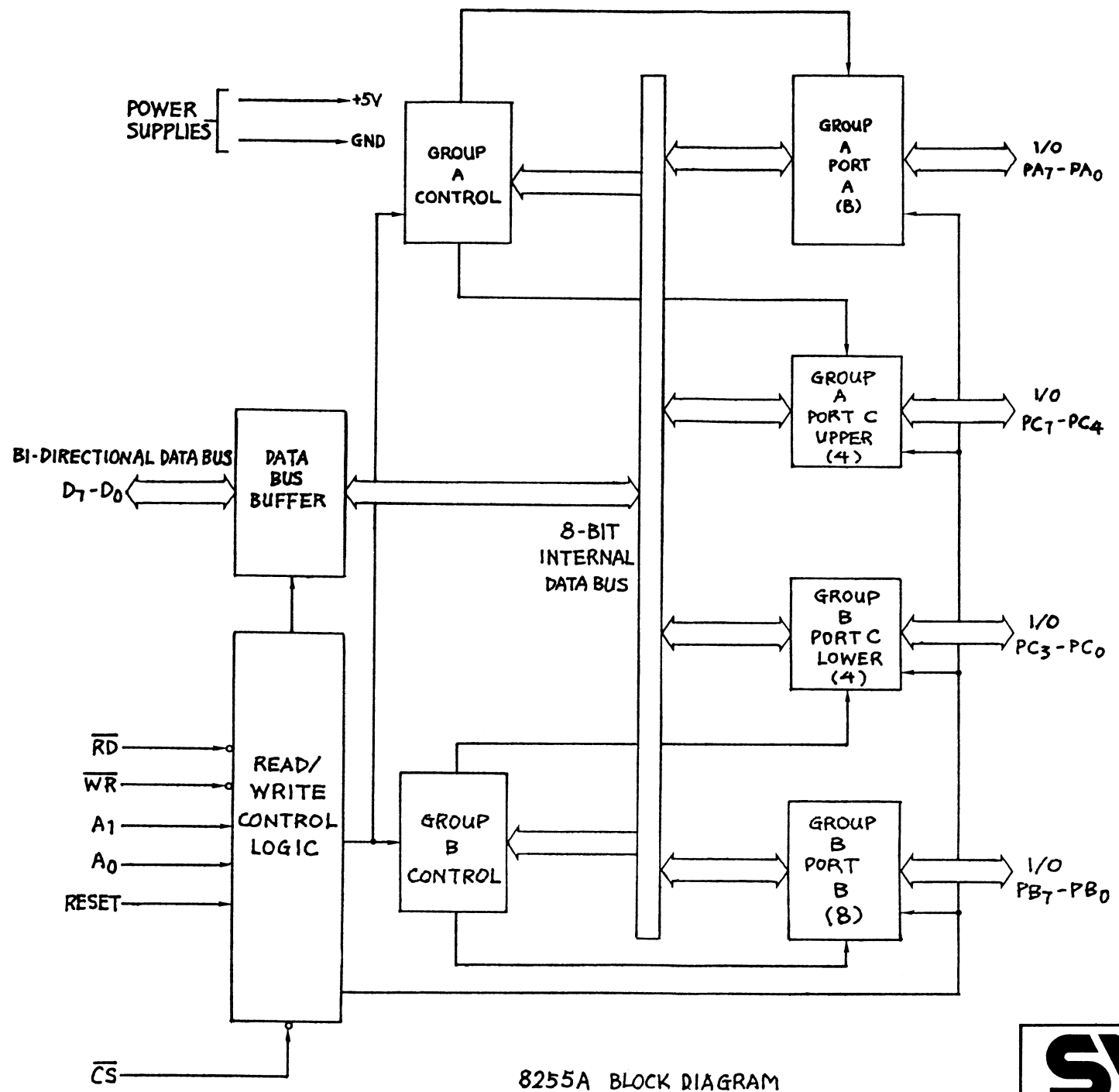


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TITLE AY-3-8910 PROGRAMMABLE SOUND GENERATOR BLOCK DIAGRAM	VERIFIED BY <u>VICKY YELUN V. Y</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO STM-025-1A	VERSION NO 1.0 SHEET OF 4



8255A BLOCK DIAGRAM

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TITLE 8255A PROGRAMMABLE PERIP - -HERAL INTERFACE BLOCK DIAGRAM	VERIFIED BY <u>VICKY YEUNG V.Y.</u> DATE <u>MARCH, 1984</u>
DOCUMENT NO <u>STM-029-A</u>	VERSION NO <u>1.0</u> SHEET OF <u>5</u>